AIM:

To familiarize with logic gate IC packages and to verify the truth tables of logic gates. Also familiarize with digital IC trainer kit.

COMPONENTS REQUIRED

DIGITAL IC TRAINER KIT: The equipment mainly used to test and set up digital circuits. Integrated circuits can be fitted in sockets or bread board. There are built in voltage sources and clock signals. In order to feed monopulses manually, a debouncer switch is also provided. A number of select switches are provided to obtain '0' or '1' state voltages as digital inputs. Green and Red LEDs are provided to represent low and high states respectively to visualize the digital outputs.

IC PACKAGES: 7404-Hex inverter gates
7400-Quad two input NAND gates
7402-Quad two input NOR gates
7408-Quad two input AND gates
7432-Quad two input OR gates
7486-Quad two input XOR gates

PROCEDURE

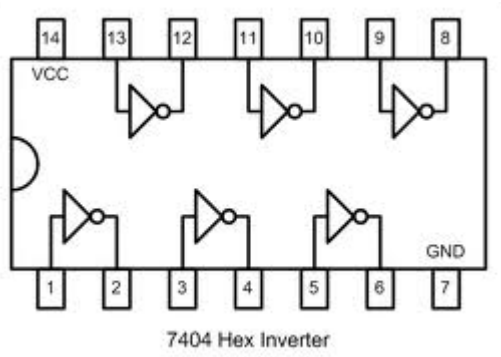
1) Test the IC using digital IC tester before conducting the experiment

2) Verify the dual in line package pin out the IC before feeding the input

3) Set up the circuit and observe the output. Enter the input and output stages in truth table corresponding to the input combinations

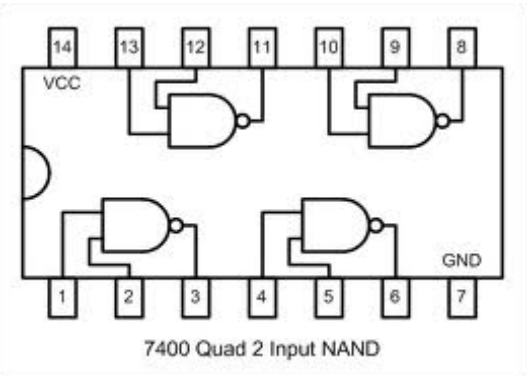
PIN CONFIGURATION AND TRUTH TABLE

1. 7404-Hex inverter gates



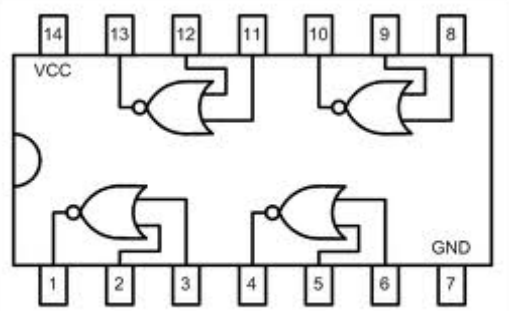
7404 Hex Inverter

2. 7400-Quad two input NAND gates



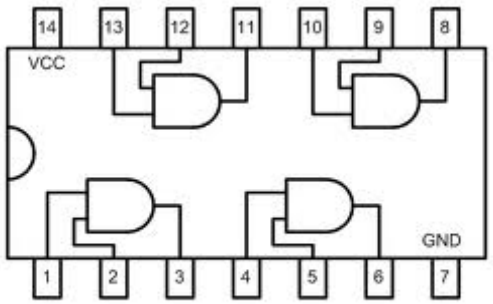
7400 Quad 2 Input NAND

3. 7402-Quad two input NOR gates



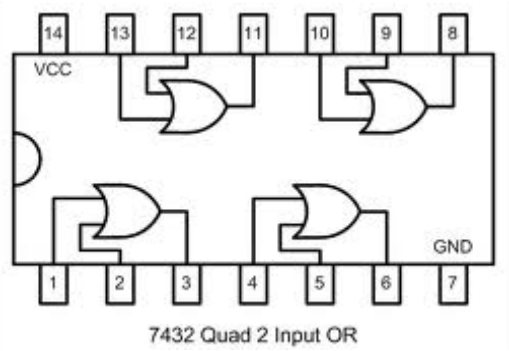
7402 Quad 2 Input NOR

4. 7408-Quad two input AND gates



7408 Quad 2 Input AND

5. 7432-Quad two input OR gates



7432 Quad 2 Input OR

RESULT

Familiarized the digital IC trainer kit &logic gate IC packages and verified the truth tables of logic gates.

	Dev Bhoomi Institute Of Technology Department of Electronics and Communication Engineering		LABORATORY MANUAL
	PRACTICAL INSTRUCTION SHEET		
	EXPERIMENT NO. 2	ISSUE NO. :	ISSUE DATE:
	REV. NO. :	REV. DATE :	PAGE: 3
LABORATORY Name & Code: **Digital Electronics**			SEMESTER: III

AIM

1. To design and set up half adder and half subtractors using

a. EXOR gates and AND gates
b. NAND gates

COMPONENTS REQUIRED

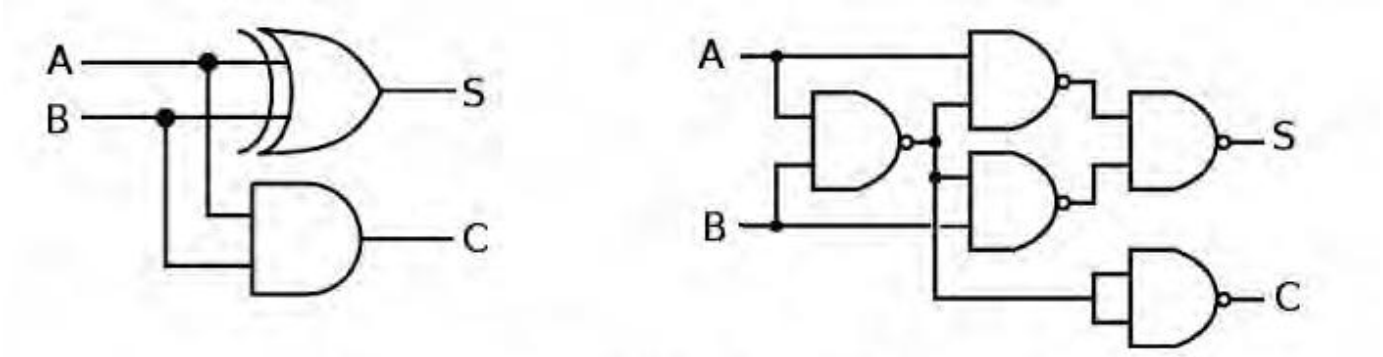
IC Trainer kit, IC 7400, IC 7486

PRINCIPLE

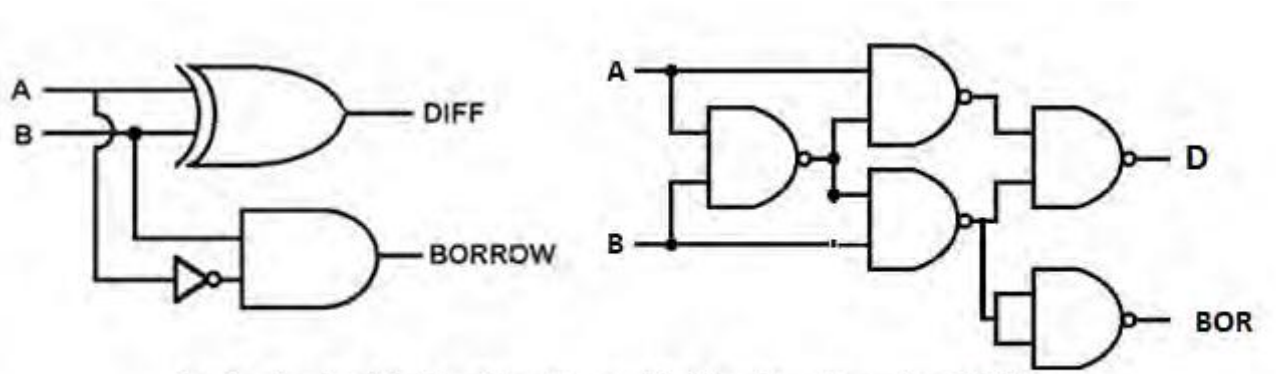
The simplest binary adder is called half adder. Half adder has two input bits and two output bits. One output bit is the sum and the other is the carry. They are represented by 'S' and 'C' respectively in logic symbol.

The simplest binary Subtractor is called half Subtractor. It has two input bits and two output bits. One output bit is the Difference and the other is borrowed. They are represented by 'D' and 'B' respectively in logic symbol

Truth table of Half Adder				**Truth table of Half Subtractor**			
Inputs		Output		Inputs		Output	
A	**B**	**S**	**C**	**A**	**B**	**D**	**BOR**
0	0	0	0	0	0	0	0
0	1	1	0	0	1	1	1
1	0	1	0	1	0	1	0
1	1	0	1	1	1	0	0



Logic circuit of Half adder and Haff adder using NAND gate only



Logic circuit of half subtractor and half subtractor using NAND gates

PROCEDURE

1. Verify whether all the wires and components are in good condition.
2. Set up a half adder circuit and feed all the input combinations.
3. Observe the output corresponding to input combinations and enter it in the Truth table.
4. Repeat the above steps for half subtractors circuits.

RESULT AND DISCUSSION

Half adder and the half subtractors circuits are set up using logic gates and verified the result

b) To design and set up full adder and full Subtractor using

a. EXOR gates and AND gates
b. NAND gates

COMPONENTS REQUIRED

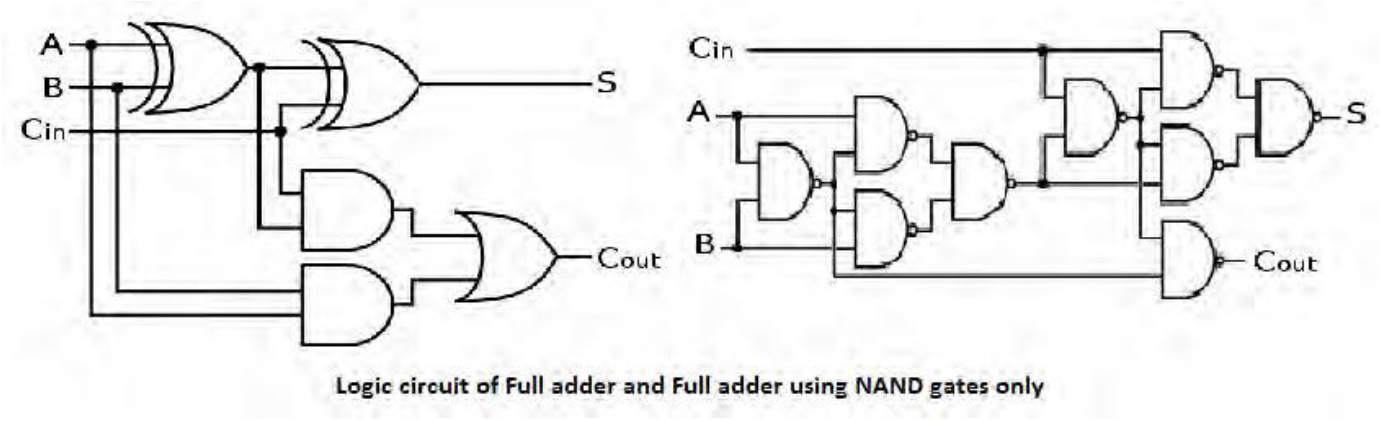
IC Trainer kit, ICS 7400, IC 7486

PRINCIPLE

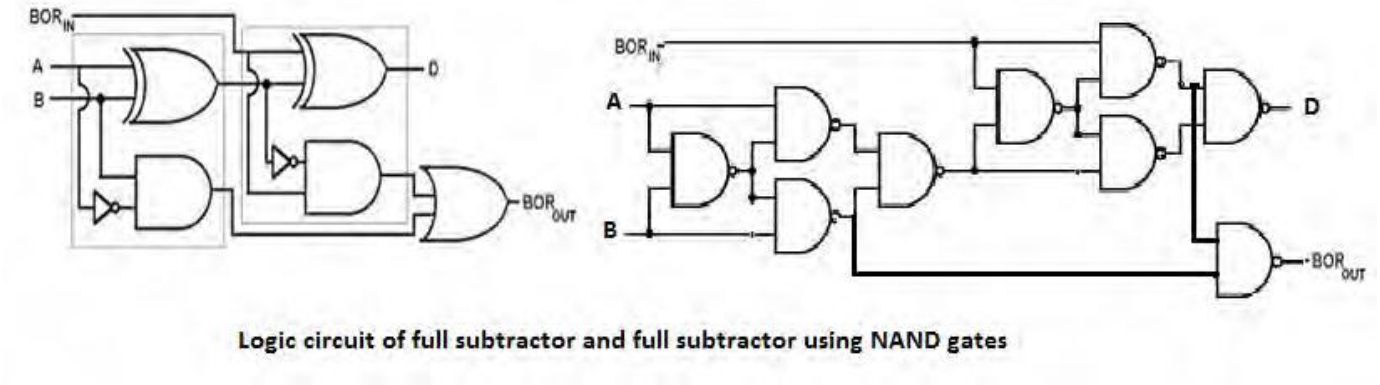
A half adder has no provision to add a carry from the lower order bits when binary numbers are added. When two input bits and a carry are to be added the number of input bits becomes three and the input combination increases to eight. For this full adder is used. Like half adder it also has a sum bit and a carry bit. The new carry generated is represented by 'Cout' and the carry generated from the previous addition is represented by 'Cin'

When two input bits and a borrow have to be subtracted the number of input bits equal to three and the input combinations increases to eight, for this a full Subtractor is used.

Truth table of Full Adder					Truth table of Full Subtractor				
Inputs			Output		Inputs			Output	
A	**B**	**Cin**	**S**	**Cout**	**A**	**B**	**BORin**	**D**	**BORout**
0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	1	1
0	1	0	1	0	0	1	0	1	1
0	1	1	0	1	0	1	1	0	1
1	0	0	1	0	1	0	0	1	0
1	0	1	0	1	1	0	1	0	0
1	1	0	0	1	1	1	0	0	0
1	1	1	1	1	1	1	1	1	1



Logic circuit of Full adder and Full adder using NAND gates only



Logic circuit of full subtractor and full subtractor using NAND gates

PROCEDURE

1. Verify whether all the wires and components are in good condition
2. Set up full adder circuit and feed all the input combinations
3. Observe the output corresponding to input combinations and enter it in the Truth table
4. Repeat the above steps for Full subtractors circuits

RESULT AND DISCUSSION

Full adder and the Full subtractors circuits are set up using logic gates and verified the result.

	Dev Bhoomi Institute Of Technology Department of Electronics and Communication Engineering		LABORATORY MANUAL
	PRACTICAL INSTRUCTION SHEET		
	EXPERIMENT NO. 3	ISSUE NO. :	ISSUE DATE:
	REV. NO. :	REV. DATE :	PAGE: 2
LABORATORY Name & Code: **Digital Electronics**			SEMESTER: III

OBJECT: Breadboard implementation of SR and D- flip flop and verify their characteristic table.

APPARATUS REQUIRED: - IC -7400, IC- 7404, and logic trainer board, connecting wires.

THEORY: S-R FLIP FLOP: -

A S R flip flop can be built using NOR gate or NAND gate .It has two inputs R and S and two O/P are Q and Q .In a flip flop the two O/Ps are complementary, If Q=1 then Q=0.A low R and low S result in inactive state (there is no change). A low R and high S results in set state while high R and low S results in reset state. If R and S are high sate, the O/P is in determined and this is called race condition.

FLIP FLOP: -

The storage elements employed in clocked sequential circuits are called flip-flop. A flip-flop is a binary storage bit of information .A flip-flop maintains a binary state until directed by clock pulse to switch states. Theory of T flip-flop is presented below.

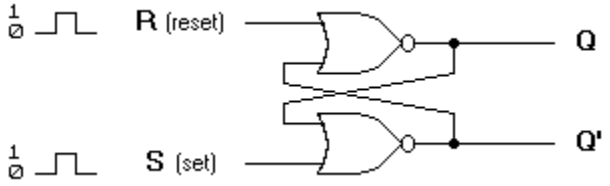
The memory elements in a sequential circuit are called flip-flops. A flip-flop circuit has two outputs, one for the normal value and one for the complement value of the stored bit. Binary information can enter a flip- flop in a variety of ways and gives rise to different types of flip-flops.

Introduction - Basic Flip-Flop Circuit

A flip-flop circuit can be constructed from two NAND gates or two NOR gates. These flip-flops are shown in Figure 2 and Figure 3. Each flip-flop has two outputs, *Q* and *Q'*, and two inputs, *set* and *reset*. This type of flip-flop is referred to as an *SR flip-flop* or *SR latch*. The flip-flop in Figure 2 has two useful states. When Q=1 and Q'=0, it is in the *set state* (or 1-state). When Q=0 and Q'=1, it is in the *clear state* (or 0-state). The outputs Q and Q' are complements of each other and are referred to as the normal and complement outputs, respectively. The binary state of the flip-flop is taken to be the value of the normal output.

When a 1 is applied to both the set and reset inputs of the flip-flop in Figure 2, both Q and Q' outputs go to 0. This condition violates the fact that both outputs are complements of each other. In normal operation this condition must be avoided by making sure that 1's are not applied to both inputs simultaneously.

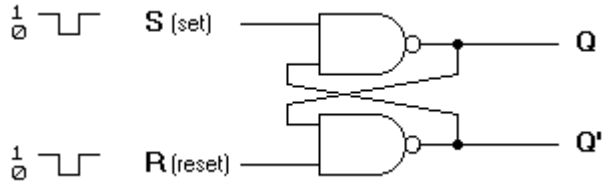
(a) Logic diagram



S R	Q Q'	
1 0	1 0	
0 0	1 0	(after S=1, R=0)
0 1	0 1	
0 0	0 1	(after S=0, R=1)
1 1	0 0	

(b) Truth table

Figure 2. Basic flip-flop circuit with NOR gates



(a) Logic diagram

S R	Q Q'	
1 0	0 1	
1 1	0 1	(after S=1, R=0)
0 1	1 0	
1 1	1 0	(after S=0, R=1)
0 0	1 1	

(b) Truth table

Figure: Basic flip-flop circuit with NAND gates

The NAND basic flip-flop circuit in Figure 3(a) operates with inputs normally at 1 unless the state of the flip-flop has to be changed. A 0 applied momentarily to the set input causes Q to go to 1 and Q' to go to 0, putting the flip-flop in the set state. When both inputs go to 0, both outputs go to 1. This condition should be avoided in normal operation.

TRUTH TABLE FOR S-R FLIP-FLOP: -

INPUT S	**INPUT R**	**OUTPUT Q (t)**	**Q (t+1)**	**COMMENT**
0	0	0	0	Previous stage
0	1	0	0	Reset
1	0	1	1	Set
1	1	1	1	In determined

TRUTH TABLE FOR S-R FLIP-FLOP: -

INPUT D	OUTPUT Q (t+1)	COMMENT
0	0	No change
1	1	Set

PROCEDURE:

1. Insert ICs according to the circuit diagram on the trainer board.
2. Give +5V supply to the pin 14 and ground to the pin 7 to all ICs.
3. Give inputs S, R and CLK to the respective pins of the ICs and observe the output at outputlogic.
4. Observe LEDs output.
5. Try with different combination of input S and R.
6. Prepare truth table, observe and verify it.

RESULT: Truth table of S-R and D flip flop are verified.

PRECAUTION:

1. All connection should be tight.
2. After all connection of the circuit, the main supply should be ON.

AIM

To design and set up four bit Johnson and ring counter using JK FF

COMPONENTS REQUIRED

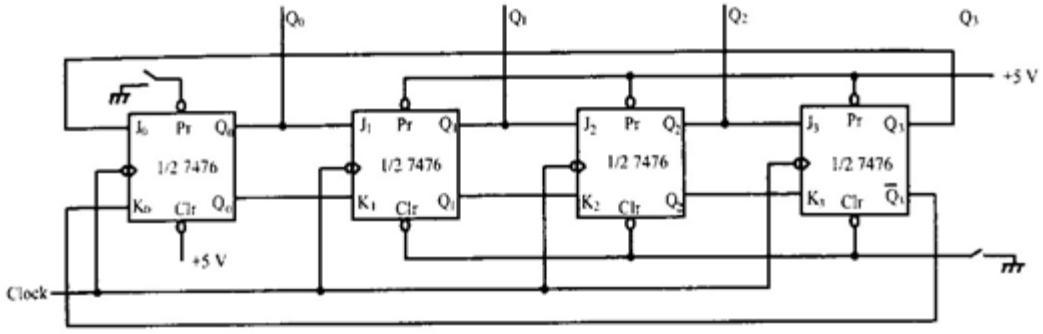
Digital IC trainer kit, IC 7476

PRINCIPLE

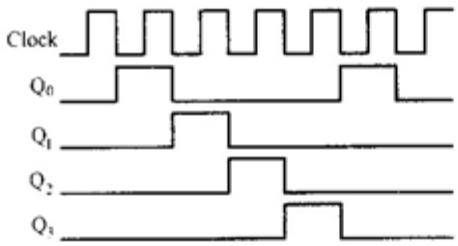
Ring counter and Johnson counters are basically shift registers

Ring counter

It is made by connecting Q&Q' output of one JK FF to J&K input of next FF respectively. The output of final FF is connected to the input of first FF. To start the counter the first FF is set by using preset facility and the remaining FF are reset input. When the clock arrives the set condition continues to shift around the ring



Waveforms for ring counter



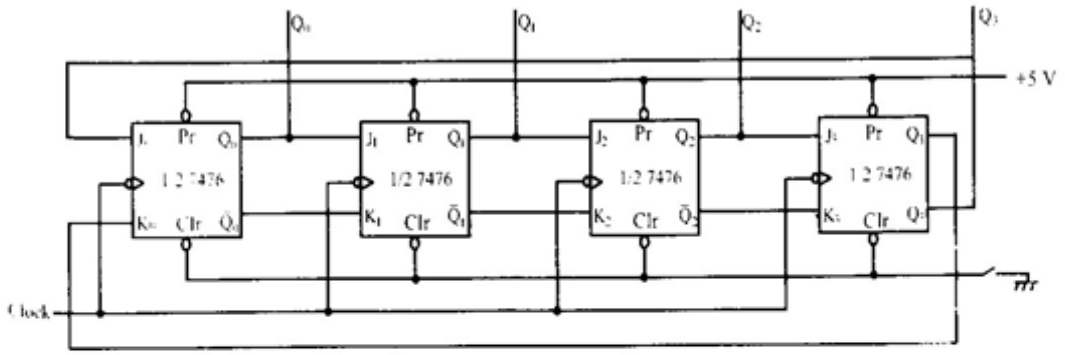
Clk	Q_0 Q_1 Q_2 Q_3
1	1 0 0 0
2	0 1 0 0
3	0 0 1 0
4	0 0 0 1

As it can be seen from the truth table there are four unique output stages for this counter. The modulus value of a ring counter is *n,* where *n* is the number of flip flops. Ring counter is called divided by N counter where N is the number of FF.

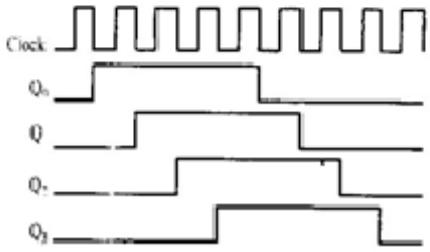
Johnson counter (Twisted ring counter)

The modulus value of a ring counter can be doubled by making a small change in the ring counter circuit. The Q' and Q of the last FFS are connected to the J and K input of the first FF respectively. This is the Johnson counter.

Johnson counter



Waveforms for Johnson counter



Clk	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

Initially the FFs are reset. After first clock pulse FF0 is set and the remaining FFs are reset. After the eight clock pulse all the FFS are reset. There are eight different conditions creating a mode 8 Johnson counter. Johnson counter is called a twisted ring counter or divide by 2N counter.

PROCEDURE

1. Set up the ring counter and set clear Q outputs using PRESET and apply mono pulse.
2. Note down the state of the ring counter on the truth table for successive clock 0.
3. Repeat the steps for Johnsons counter

RESULT AND DISCUSSION

Four bit ring counter and the Johnson counter were set up using the JK FF and verified.

OBJECT: -Breadboard implementation of Shift Register.

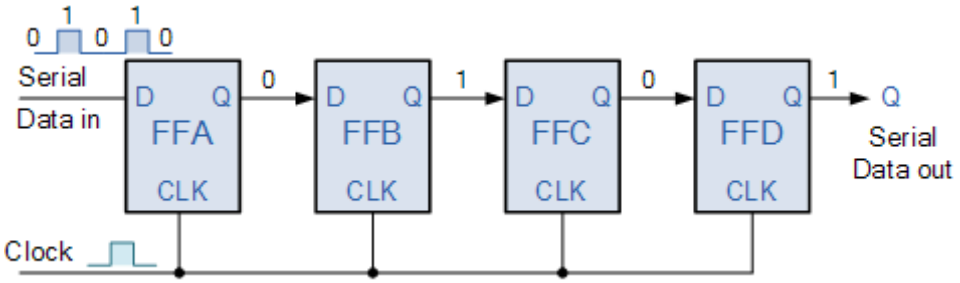
APPARATUS USED: -

1. General-purpose trainer board.
2. Ic7491- Serial In Parallel Out
3. Ic74164- Serial In Parallel Out
4. Ic74165 – Parallel In Serial Out
5. Ic74194- Parallel In Parallel Out
6. Patch Cords

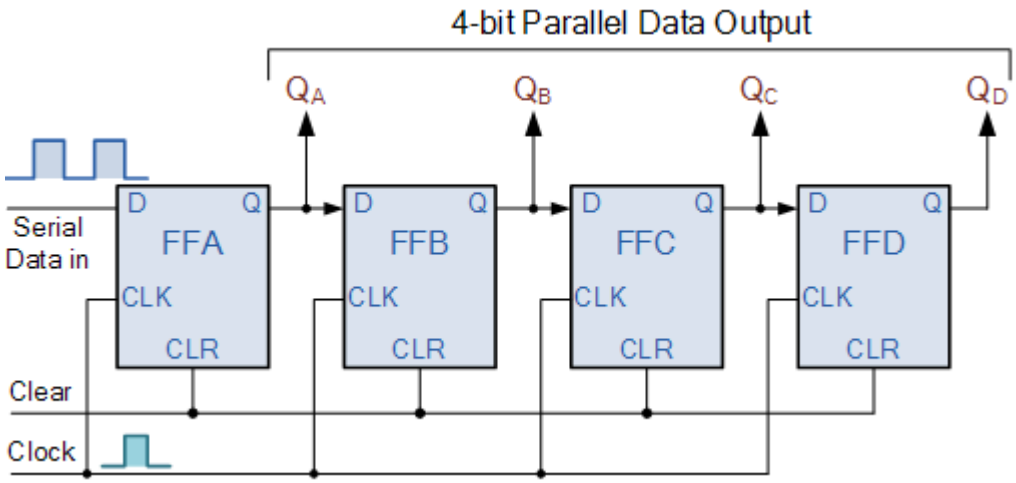
THEORY: - A register is simply a group of flip-flop that can be used to store a binary no. of a group of Flip- flop connected to provide either or both of these function is called shift register. To allow the data in the word to read in to the register serially. The o/p of the flip-flop is connected to the i/p of the following binary such a configuration called a Shift register.

There are two ways to shift the data into a register (serial and parallel) and similarly two ways to shift the data out of the register. This leads to construction of four types of registers.

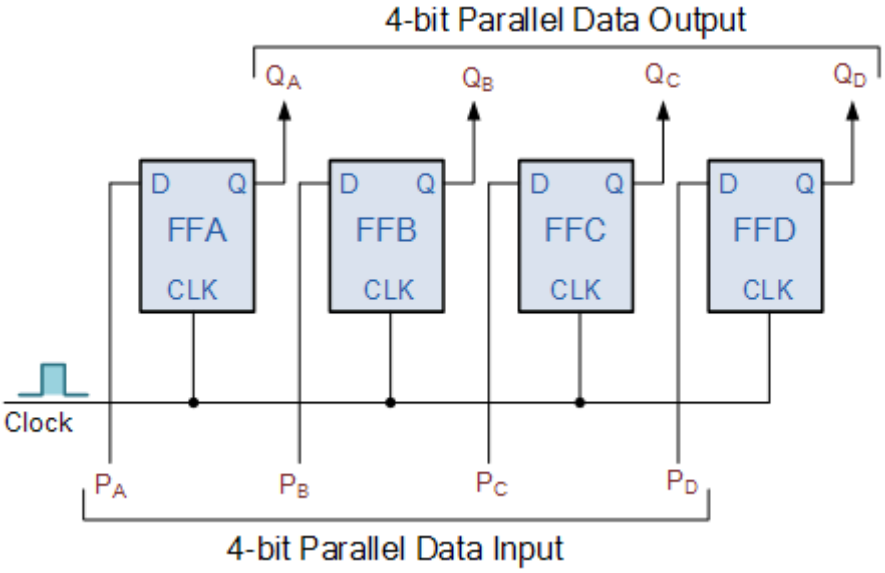
1. SISO



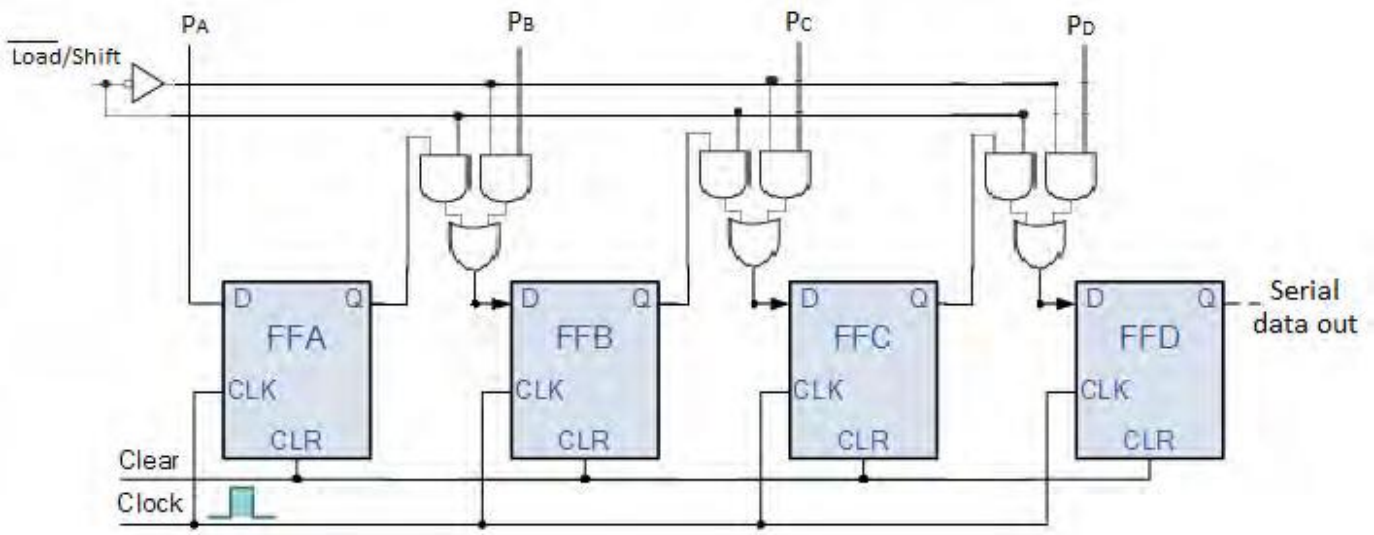
2. Serial In Parallel Out (SIPO)



3. Parallel In Parallel Out (PIPO)



4. Parallel In Serial Out (PISO)



RESULT:- All Shift Register Verify With the given truth table.

PRECAUTIONS: -

1. Connection should be tight.
2. O/P should be finding sequentially.
3. IC's should be handled carefully.

	Dev Bhoomi Institute Of Technology Department of Electronics and Communication Engineering		LABORATORY MANUAL
	PRACTICAL INSTRUCTION SHEET		
	EXPERIMENT NO. 6	ISSUE NO. :	ISSUE DATE:
	REV. NO. :	REV. DATE :	PAGE: 2
LABORATORY Name & Code: **Digital Electronics**			SEMESTER: III

EXPERIMENT: Implementation of arithmetic algorithms.

APPARATUS REQUIRED:

S.No.	Equipment	Qty.
1	General purpose digital trainer	1
2	IC-74181	1

THEORY: - Arithmetic logic unit is a multipurpose device capable of providing several different arithmetic and logic operations. The specific operation to be performed is selected by the user by placing a specific binary code on the mode select i/p. ALU s are available in large scale integrated circuit packages.

Functional block diagram For 74181 ALU is shown in fig. It is a 4-bit ALU, which provides 16 arithmetic plus 16 logic operations. The unit accepts two 4-bit words (A_3 A_2 A_1 A_0 and B_3 B_2 $B_{1\ B0)}$ and a carry i/p Cn as i/p's.

The operation to be performed on these i/p are determined by logic levels on i/ps

PROCEDURE:

1. Put IC on the breadboard.
2. Apply Vcc supply at pin 24.
3. Apply ground at pin 12.
4. Make connections as shown in the circuit diagram.
5. Observe the different outputs.

OBSERVATION TABLE:

SELECTION				M=1 LOGIC FUNCTION	M=0 ARITHMRTIC OPERATION
S_3	S_2	S_1	S_0		
0	0	0	0	F=A	F=A
0	0	0	1	F=A+B	F=A+B
0	0	1	0	F=AB	F=A+B
0	0	1	1	F=0	F= -1
0	1	0	0	F=AB	F=A+AB
0	1	0	1	F=B	F=(A+B)+ AB
0	1	1	0	F=A O B	F=A – B -1
0	1	1	1	F=AB	F=AB -1
1	0	0	0	F=A+B	F=A + AB
1	0	0	1	F=A O B	F=A+B
1	0	1	0	F=B	F= (A+B) + AB
1	0	1	1	F=AB	F=AB -1

1	1	0	0	F=1	A + A*
1	1	0	1	F=A+B	F=(A+B) +A
1	1	1	0	F=A+B	F=(A+B) +A
1	1	1	1	F=A	F=A - 1

RESULT: The functional table is verified for 74181 IC.

PRECAUTIONS: -

1. Connection should be tight.
2. O/P should be finding sequentially.
3. IC's should be handled careful

AIM

To design Multiplexer and Demultiplexer and verify their truth tables.

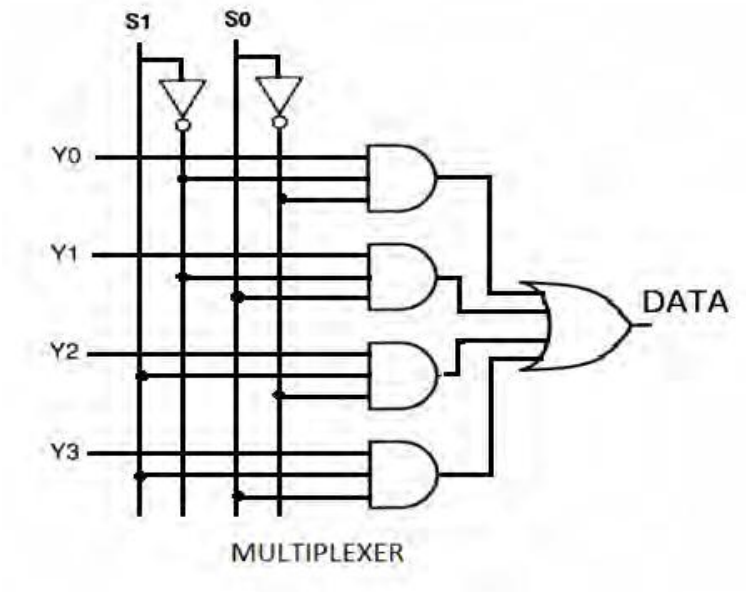
COMPONENTS REQUIRED: -

Digital IC trainer kit, IC

PRINCIPLE

In electronics, a multiplexer (or mux) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2*n* inputs has *n* select lines, which are used to select which input line to send to the output. An electronic multiplexer can be considered as a multiple-input, single-output switch. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. A multiplexer is also called a data selector.

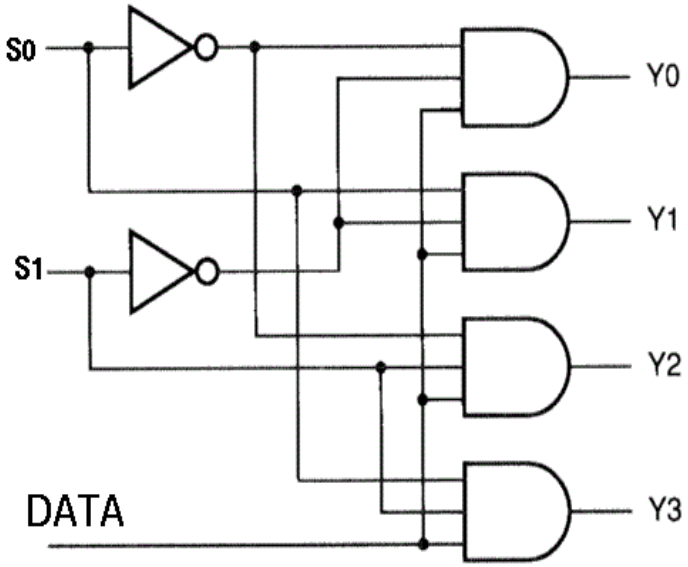
Conversely, a Demultiplexer (or Demux) is a device taking a single input signal and selecting one of many data-output-lines, which is connected to the single input. An electronic Demultiplexer can be considered as a single-input, multiple-output switch. A multiplexer is often used with a complementary Demultiplexer on the receiving end.



MULTIPLEXER

S1	S0	DATA
0	0	Y0
0	1	Y1
1	0	Y2
1	1	Y3

DB27



DEMULTIPLEXER

TRUTH TABLE						
INPUTS			OUTPUTS			
DATA	S1	S0	Y3	Y2	Y1	Y0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

PROCEDURE:

1. Connections are made as per the circuit diagram
2. Switch on the power supply
3. Apply different combinations of inputs and observe the outputs; compare the outputs with the truth tables.

RESULT:

Multiplexer and Demultiplexer are constructed and verified the truth tables.

AIM

To design and set up the circuit of BCD to Excess-3 converter.

COMPONENTS REQUIRED

IC Trainer kit IC 7486, IC 7408, IC 7404, IC 7432

PRINCIPLE

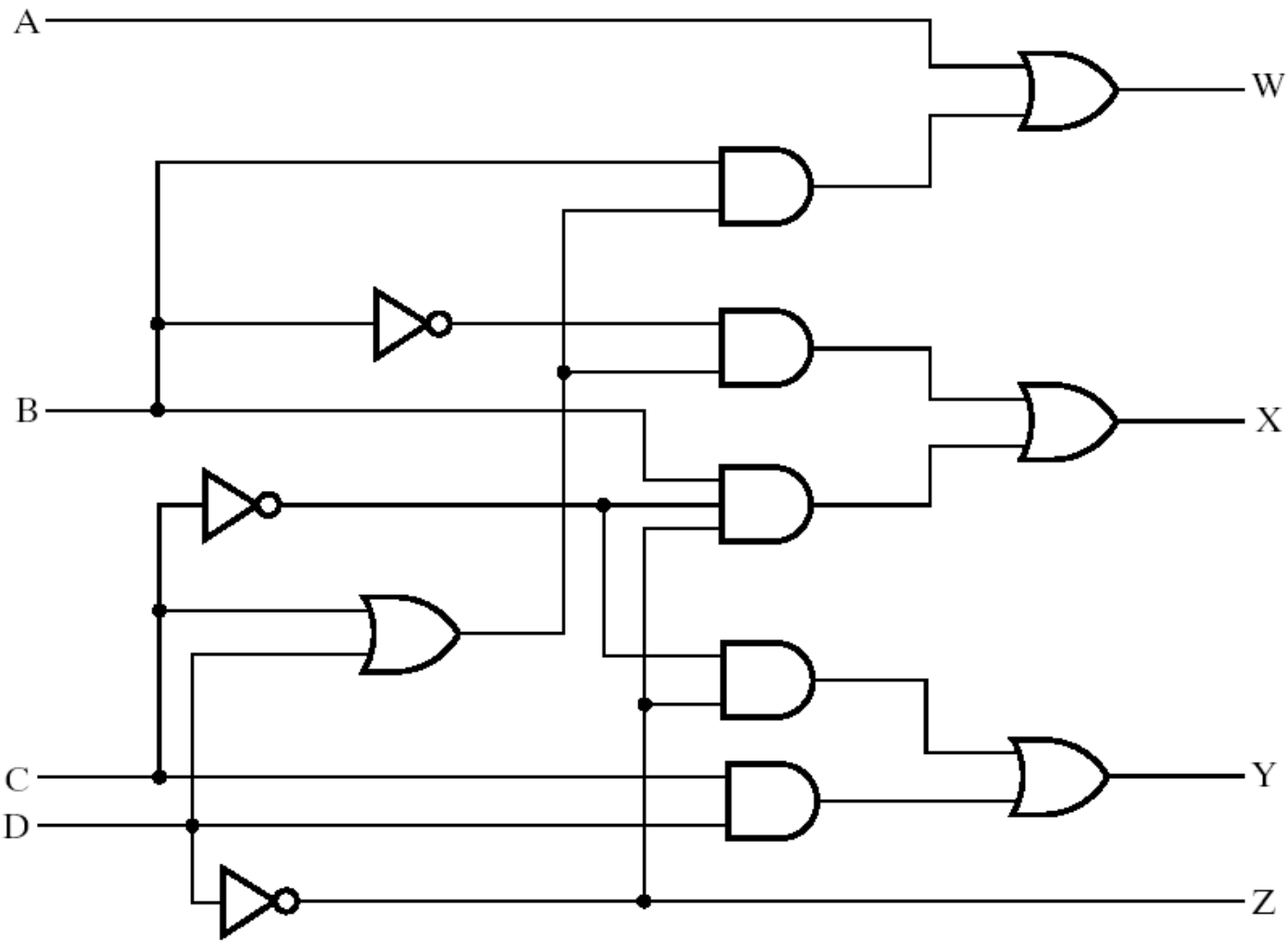
The Excess-3code for a decimal digit is the binary combination corresponding to the decimal digit plus 3. For example, the excess-3 code for decimal digit 5 is the binary combination for 5+3=8, which is 1000.Each BCD digit four bits with the bits with the bits, from most significant to least significant, labeled A,B,C,D. As the same for excess-3

PROCEDURE

1. Test all the components using multi meter and digital IC tester
2. Verify the truth table of the circuit by feeding input bit combinations

Truth Table - BCD to Excess-3 code

Decimal Digit	Input BCD				Output Excess-3			
	A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0



RESULT

The circuit of BCD to Excess-3 converter has set up and verified the result